USB2811

User's Manual

Beijing ART Technology Development Co., Ltd.

Contents

Chapter 1 Overview

In the fields of Real-time Signal Processing, Digital Image Processing and others, high-speed and high-precision data acquisition modules are demanded. ART USB2811 data acquisition module, which brings in advantages of similar products that produced in china and other countries, is convenient for use, high cost and stable performance.

ART USB2811 is a data acquisition module based on USB bus. It can be directly inserted into computer's USB interface which is compatible with USB2811 to constitute the laboratory, product quality testing center and systems for different areas of data acquisition, waveform analysis and processing. It may also constitute the monitoring system for industrial production process.

Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.
Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

➢ USB2811 Data Acquisition Board
➢ ART Disk
  a) user's manual (pdf)
  b) drive
  c) catalog
➢ Warranty Card

FEATURES

Analog Input

➢ Converter Type: AD7663ASTZ (AD7663(default), and AD7665)
➢ Input Range: ±10V, ±5V, ±2.5, 0~10V, 0~5V
➢ 16-bit resolution
➢ Sampling Rate: 31Hz~250KHz (when use AD7665, Sampling Rate: 31Hz~500KHz)
➢ Analog Input Mode: 16SE/8DI
➢ Data Read Mode: non-empty, half-full inquiry mode
➢ Memory Depth: 8K word FIFO memory
➢ Memory Signs: non-empty and half-full
➢ AD Mode: continuum sampling , grouping sampling
➢ Group Interval: software-configurable, minimum value is sampling period, maximum value is 32767uS
➢ Loops of Group: software-configurable, minimum value is one time , maximum value is 255 times
➢ Clock Source: external clock, internal clock (software-configurable)
➢ Trigger Mode: software trigger, hardware trigger (external trigger)
➢ Trigger Type: level trigger , edge trigger
➢ Trigger Direction: negative, positive, either positive or negative trigger
➢ Trigger Source: ATR, DTR
➢ Trigger Source ATR Input Range: -10V~10V

- ➢ Trigger Source DTR Input Range: standard TTL level
- ➢ Programmable Gain: 1, 2, 4, 8 (AD8251 default)or 1, 2, 5, 10 (AD8250) or 1, 10, 100, 1000 (AD8253)
- ➢ Analog Input Impedance: 10MΩ
- ➢ Amplifier Set-up Time: 785nS(0.001%)(max)
- ➢ AD Conversion Time: 1.25uS
- ➢ Non-linear error: ±1LSB(Maximum)
- ➢ System Measurement Accuracy: 0.01%
- ➢ Operating Temperature Range: 0℃~55℃
- ➢ Storage Temperature Range: −20℃~70℃

Analog Output

- ➢ Converter Type: AD5725
- ➢ Output Range: ±10V,±5V (default), 0~10V, 0~5V
- ➢ 12-bit resolution
- ➢ Set-up Time: 10μS (0.01%)
- ➢ Channel No.: 4-channel
- ➢ Non-linear error: ±1LSB(Maximum)
- ➢ Output Error (full-scale): ±1LSB
- ➢ Operating Temperature Range: 0℃~55℃
- ➢ Storage Temperature Range: −20℃~70℃

Digital Input

- ➢ Channel No.: 16-channel
- ➢ Electric Standard: TTL compatible
- ➢ High Voltage: ≧2V
- ➢ Low Voltage: ≦0.8V

Digital Output

- ➢ Channel No.: 16-channel
- ➢ Electrical Standard: TTL compatible
- ➢ High Voltage: ≧3.8V
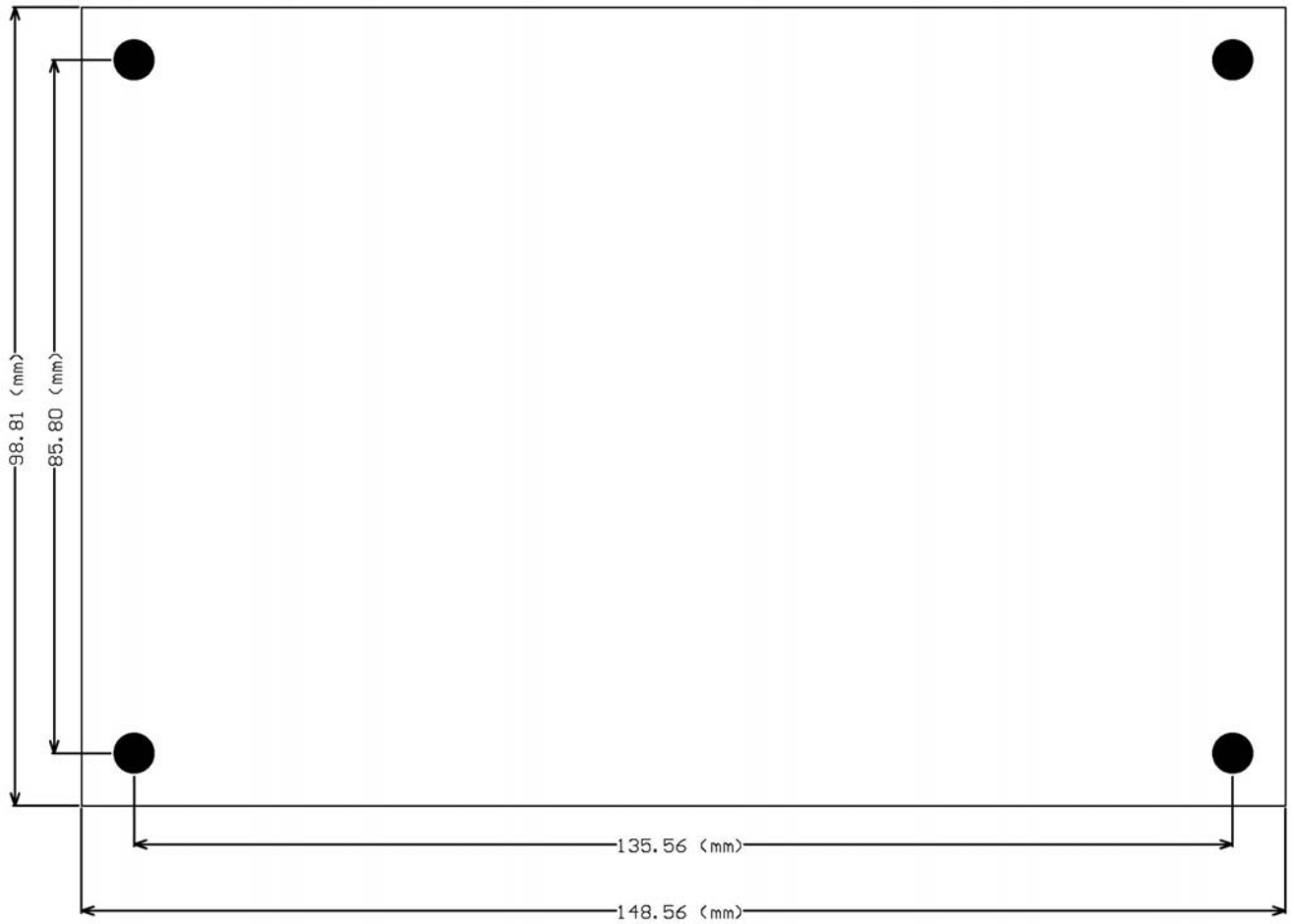- ➢ Low Voltage: ≦0.44V

CNT Counter/timer

- ➢ Channel No.: three independent subtractive counter
- ➢ 32-bit counter/timer
- ➢ Count Mode: six modes (software-configurable)
- ➢ Electrical Standard: TTL compatible
- ➢ Gate: rising edge, high level, low level
- ➢ Counter Output: high level, low level

Other features

Board Clock Oscillation: 40MHz

Dimension

148.56mm (L) x 98.81mm (W) x 16mm (H)

Chapter 2 Components Layout Diagram and a Brief Description

2.1 The Main Component Layout Diagram
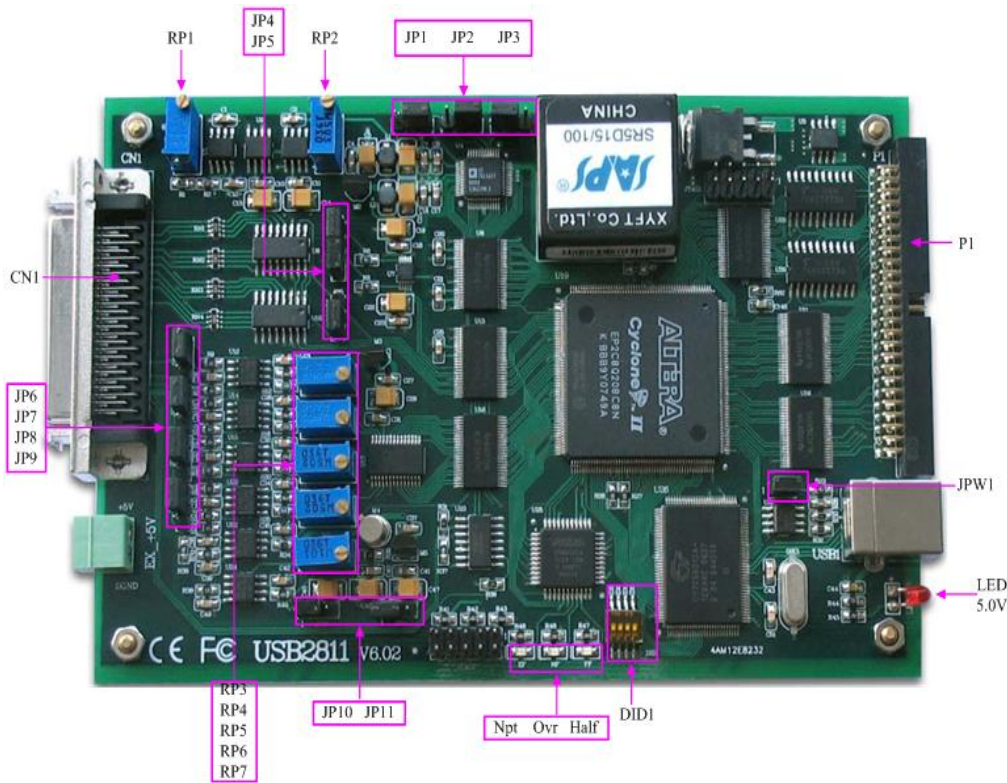
2.2 The Function Description for the Main Component

2.2.1 Signal Input and Output Connectors

CN1: Analog input and output connector

P1:   Digital signal, timer/counter signal input and output connector

2.2.2 Potentiometer

RP1:   Analog signal input zero-point adjustment potentiometer

RP2:   Analog signal input full-scale adjustment potentiometer

RP7:   AO0~AO3 analog signal output zero-point adjustment potentiometer

RP6:   AO0 analog signal output full-scale adjustment potentiometer

RP5:   AO1 analog signal output full-scale adjustment potentiometer

RP4:   AO2 analog signal output full-scale adjustment potentiometer

RP3:   AO3 analog signal output full-scale adjustment potentiometer

2.2.3 Jumper

JP1, JP2, and JP3: Analog signal input range selection
JP4, JP5: Analog signal input single-ended, double-end selection
JP10, JP11: AO0 ~ AO3 analog signal output unipolarity, bipolarity selection
JP9, JP8, JP7, JP6: AO0 ~ AO3 analog signal output range selection
JPW1: load USB controller program, 1-2 pins shorted (default)

Analog signal input range selection

Range Selection	JP1	JP2	JP3
±10V			
±5V			
±2.5V			
0~10V			
0~5V			

Analog input single-ended and double-ended selection

Selection	JP4	JP5
SE		
DI		

Analog signal output range selection

Range Selection	JP10	JP11	JP9(AO0) JP8(AO1) JP7(AO2) JP6(AO3)
0~5V			
0~10V			
±5V			
±10V			

2.2.4 Status indicator

EF: FIFO non-empty state indicator
HF: FIFO half-full status indicator
FF: FIFO overflow status indicator
LED5.0V: 5.0V power indicator, on for normal condition.

2.2.5 Physical ID of DIP Switch

DID1: Set physical ID number. When the PC is installed more than one USB2811 , you can use the DIP switch to set a physical ID number for each board, which makes it very convenient for users to distinguish and visit each board in the progress of the hardware configuration and software programming. The following four-byte numbers are expressed by the binary system: When DIP switch points to "ON", that means "1", and when it points to the other side, that means "0." As they are shown in the following diagrams: byte "ID3" is the high byte."ID0" is the low byte, and the black part in the diagram represents the location of the switch. (Test softwares of the company often use the logic ID management equipments and at this moment the physical ID DIP switch is invalid. If you want to use more than one kind of the equipments in one and the same system at the same time, please use the physical ID as much as possible. As for the differences between logic ID and physical ID, please refer to the function explanations of "CreateDevice" and "CreateDeviceEx" of *The Prototype Explanation of Device Object Management Function* in *USB2811S* software specification).
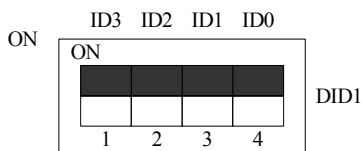
The above chart shows"1111", so it means that the physical ID is 15.
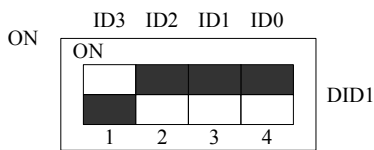
The above chart shows"0111", so it means that the physical ID is 7.
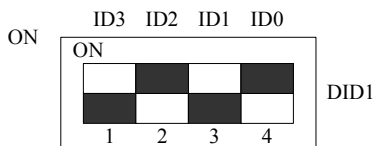
The above chart shows"0101", so it means that the physical ID is 5.

ID3	ID2	ID1	ID0	Physical ID（Hex）	Physical ID（Dec）
OFF（0）	OFF（0）	OFF（0）	OFF（0）	0	0
OFF（0）	OFF（0）	OFF（0）	ON（1）	1	1
OFF（0）	OFF（0）	ON（1）	OFF（0）	2	2

OFF（0）	OFF（0）	ON（1）	ON（1）	3	3
OFF（0）	ON（1）	OFF（0）	OFF（0）	4	4
OFF（0）	ON（1）	OFF（0）	ON（1）	5	5
OFF（0）	ON（1）	ON（1）	OFF（0）	6	6
OFF（0）	ON（1）	ON（1）	ON（1）	7	7
ON（1）	OFF（0）	OFF（0）	OFF（0）	8	8
ON（1）	OFF（0）	OFF（0）	ON（1）	9	9
ON（1）	OFF（0）	ON（1）	OFF（0）	A	10
ON（1）	OFF（0）	ON（1）	ON（1）	B	11
ON（1）	ON（1）	OFF（0）	OFF（0）	C	12
ON（1）	ON（1）	OFF（0）	ON（1）	D	13
ON（1）	ON（1）	ON（1）	OFF（0）	E	14
ON（1）	ON（1）	ON（1）	ON（1）	F	15

Chapter 3 Signal Connectors

3.1 The Definition of Analog Signal Input and Output Connector

50 core plug on the CN1 pin definition

AI0	50		25	AI1
AI2	49		24	AI3
AI4	48		23	AI5
AI6	47		22	AI7
AI8	46		21	AI9
AI10	45		20	AI11
AI12	44		19	AI13
AI14	43		18	AI15
NC	42		17	NC
NC	41		16	NC
NC	40		15	NC
NC	39		14	NC
NC	38		13	NC
NC	37		12	NC
NC	36		11	NC
NC	35		10	NC
AO0	34		9	AO1
AO2	33		8	AO3
NC	32		7	NC
NC	31		6	NC
AGND	30		5	ATR
AGND	29		4	AGND
CLKOUT	28		3	DTR
DGND	27		2	CLKIN
DGND	26		1	DGND
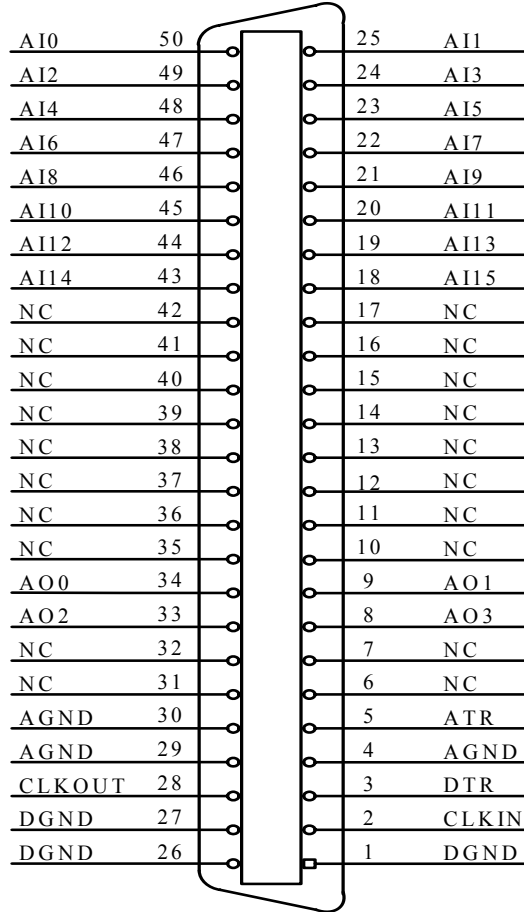
Pin definition about CN1:

Pin name	Type	Pin function definition
AI0~AI15	Input	AD analog input, reference ground is AGND.
AO0~AO3	Output	DA analog output.
AGND	GND	Analog ground. This AGND pin should be connected to the system's AGND plane.
DGND	GND	Digital ground. Ground reference for Digital circuitry. This DGND pin should be connected to the system's DGND plane.
CLKIN	Input	External clock input
CLKOUT	Output	Internal clock output
ATR	Input	Analog trigger signal input, reference ground is AGND.
DTR	Input	Digital trigger signal input, reference ground is DGND.
NC		Not Connection

3.2 The Definition of Digital Signal Input and Output Connector

50 core plug on the P1 pin definition

D O 0	1		2	D O 1
D O 2	3		4	D O 3
D O 4	5		6	D O 5
D O 6	7		8	D O 7
D O 8	9		10	D O 9
D O 10	11		12	D O 11
D O 12	13		14	D O 13
D O 14	15		16	D O 15
D G N D	17		18	D G N D
D I 0	19		20	D I 1
D I 2	21		22	D I 3
D I 4	23		24	D I 5
D I 6	25		26	D I 7
D I 8	27		28	D I 9
D I 10	29		30	D I 11
D I 12	31		32	D I 13
D I 14	33		34	D I 15
D G N D	35		36	D G N D
O U T 0	37		38	G A T E 0
C L K 0	39		40	O U T 1
G A T E 1	41		42	C L K 1
O U T 2	43		44	G A T E 2
C L K 2	45		46	D G N D
D G N D	47		48	C L K
+ 5 V	49		50	+ 5 V

Pin definition about P1:

Pin name	Type	Pin function definition
DI0~DI15	Input	Digital input
DO0~DO15	Output	Digital output
CLK0~CLK2	Input	Counter/timer output, DGND for reference ground.
GATE0~GATE2	Input	Counter/timer gate input, reference ground is DGND.
OUT0~OUT2	Output	Counter/timer output, DGND for reference ground.
CLK	Output	2MHz clock oscillator pulse output, the output period is 0.5 microseconds
DGND	GND	Digital signals ground

Chapter 4 Connection Ways for Each Signal

4.1 Analog Input Single-ended Connection

Single-ended mode can achieve a signal input by one channel, and several signals use the common reference ground. This mode is widely applied in occasions of the small interference and relatively many channels.
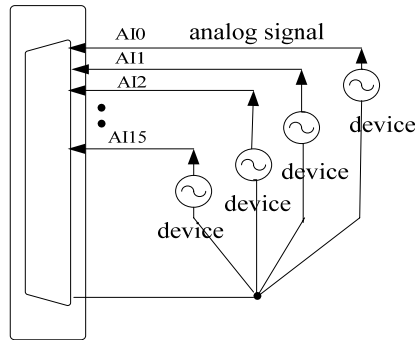

Figure 4.1 single-ended input connection

4.2 Analog Input Differential-ended Mode

Double-ended input mode, which was also called differential input mode, uses positive and negative channels to input a signal. This mode is mostly used when biggish interference happens and the channel numbers are few. Single-ended/double-ended mode can be set by the software, please refer to USB2811 software manual.

According to the diagram below, USB2811 board can be connected as analog voltage double-ended input mode, which can effectively suppress common-mode interference signal to improve the accuracy of acquisition. Positive side of the 16-channel analog input signal is connected to AI0~AI7, the negative side of the analog input signal is connected to AI8~AI15, equipments in industrial sites share the AGND with USB2811 board.
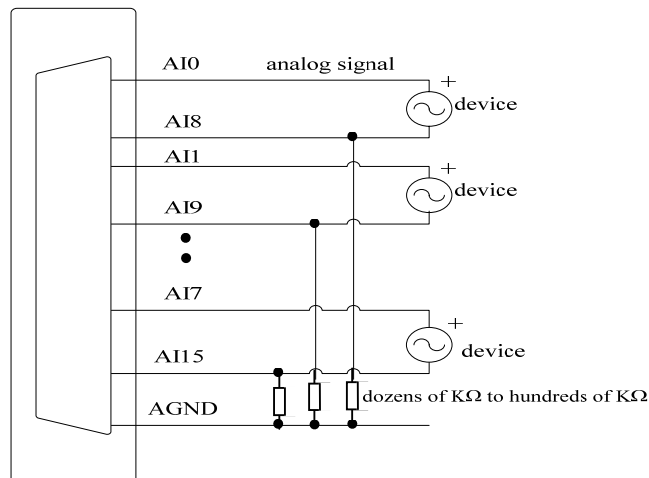

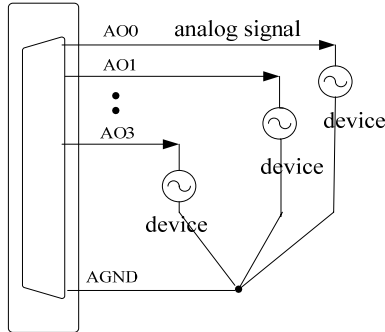*Figure 4.2 double-ended input connection*

4.3 Other Connections

Figure 4.3 analog signal output connection
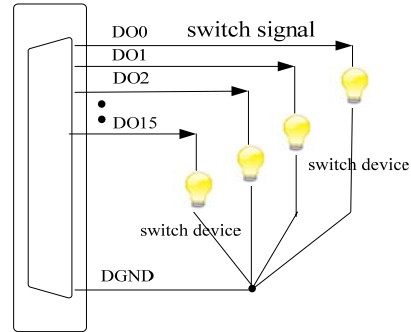

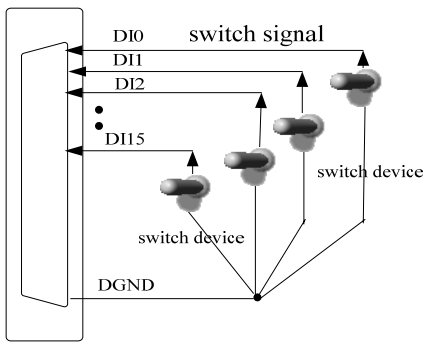*Figure 4.6 digital signal output connection*

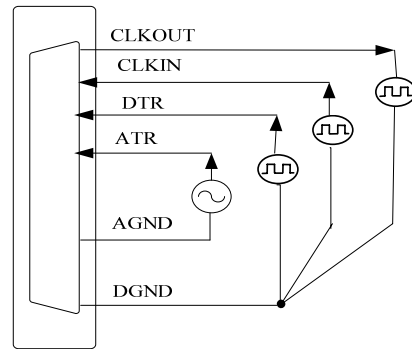*Figure 4.4 digital signal input connection*

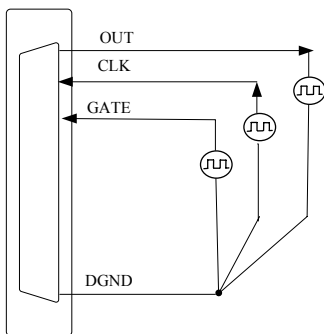*Figure 4.7 Clock Input/Output and Trigger Signal Connection*

Figure 4.5 Timer/Counter Signals connection

4.4 Methods of Realizing the Multi-card Synchronization

Three methods can realize the synchronization for the USB2811, the first method is using the cascade master-slave card, the second one is using the common external trigger, and the last one is using the common external clock.

When using master-slave cascade card programs, the master card generally uses the internal clock source model, while the slave card uses the external clock source mode. After the master card and the slave card are initialized according to the corresponding clock source mode. At first, start all the slave cards, as the main card

has not been activated and there is no output clock signal, so the slave card enters the wait state until the main card was activated. At this moment, the multi-card synchronization has been realized. When you need to sample more than channels of a card, you could consider using the multi-card cascaded model to expand the number of channels.
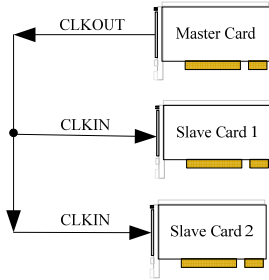

When using the common external trigger, please make sure all parameters of different USB2811 are the same. At first, configure hardware parameters, and use analog or digital signal triggering (ATR or DTR), then connect the signal that will be sampled by USB2811, input triggering signal from ART pin or DTR pin, then click "Start" button, at this time, USB2811 does not sample any signal but waits for external trigger signal. When each module is waiting for external trigger signal, use the common external trigger signal to startup modules, at last, we can realize synchronization data acquisition in this way. See the following figure:
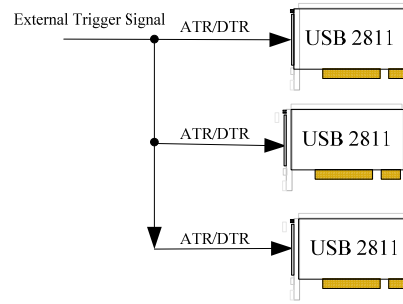
When using the common external clock trigger, please make sure all parameters of different USB2811 are the same. At first, configure hardware parameters, and use external clock, then connect the signal that will be sampled by USB2811, input trigger signal from ART pin or DTR pin, then click "Start" button, at this time, USB2811 does not sample any signal, but wait for external clock signal. When each module is waiting for external clock signal, use the common external clock signal to startup modules, at last, we realize synchronization data acquisition in this way. See the following figure:
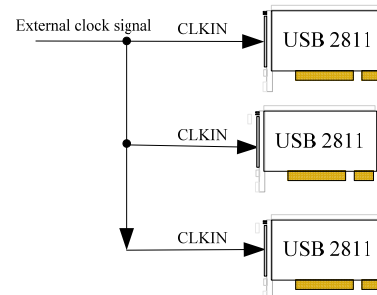
Chapter 5 The Instruction of the Trigger Function

5.1 Internal Trigger Mode

When A/D is in the initialization, if the hardware parameter ADPara.TriggerMode = USB2811_TRIGMODE_SOFT, we can achieve the internal trigger acquisition. In this function, when calling the InitDeviceAD function, it will generate A/D start pulse, AI immediately access to the conversion process and not wait for the conditions of any other external hardware. It also can be interpreted as the software trigger.

As for the specific process, please see the figure below, the cycle of the A/D work pulse is decided by the sampling frequency.
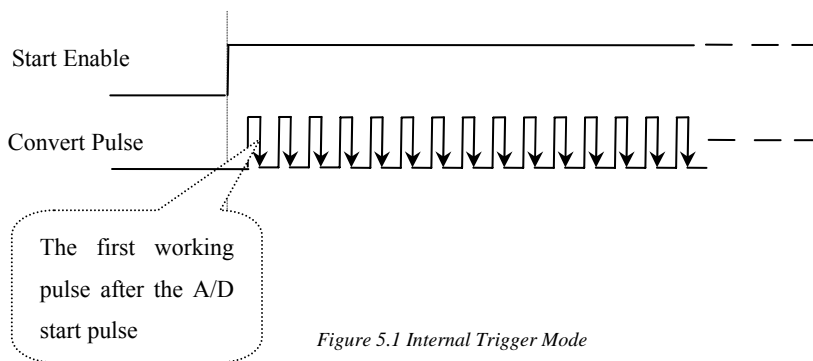

Figure 5.1 Internal Trigger Mode

The first working pulse after the A/D start pulse

5.2 External Trigger Mode

When A/D is in the initialization, if the hardware parameter ADPara.TriggerMode = USB2811_TRIGMODE_POST, we can achieve the external trigger acquisition. In this function, when calling the InitDeviceAD function, A/D will not immediately access to the conversion process but wait for the external trigger source signals accord with the condition, then start converting the data. It also can be interpreted as the hardware trigger. Trigger source includes the DTR (Digital Trigger Source) and ATR (Analog Trigger Source)

（一） **ATR Trigger**

Analog trigger uses a certain range of analog signal as a trigger source. ATR trigger source signal and the analog trigger level signal into the analog comparator at the same time, in comparator they will do a high-speed analog compare, to generate a desired comparison result to trigger A/D converter. Analog trigger level signal is decided by the AO0.

(1) Edge trigger function

Edge trigger is to capture the characteristics of the changes between the trigger source signal and the trigger level signal to trigger A/D conversion.

When ADPara.TriggerDir = USB2811_TRIGDIR_NEGATIVE, choose the trigger mode as the falling edge trigger. That is, when the ATR trigger signal is lower than trigger level, A/D will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition.
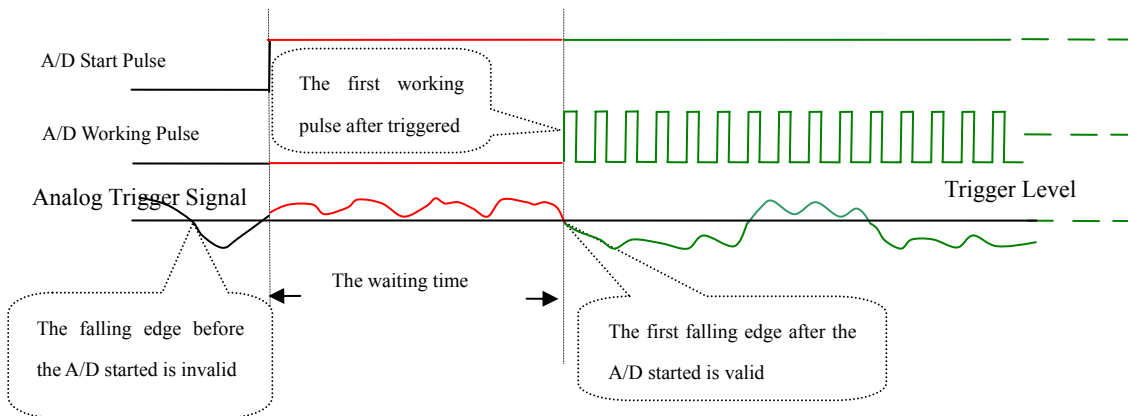
Figure5.2 Analog Trigger Source，Falling edge Trigger

When ADPara.TriggerDir = USB2811_TRIGDIR_POSITIVE, choose the trigger mode as rising edge trigger. That is, when the ATR trigger signal is higher than trigger level, A/D will immediately access to the conversion process, and its follow-up changes have no effect on AI acquisition.

When ADPara.TriggerDir = USB2811_TRIGDIR_POSIT_NEGAT, choose the trigger mode as rising or falling edge trigger. That is, when the ATR trigger signal is across the trigger level, AI will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition. This function can be used in the case that the acquisition will occur if the exoteric signal changes.

（2）**Level trigger function**

Level trigger is to capture the condition that trigger signal is higher or lower than the trigger level to trigger A/D conversion.
When ADPara.TriggerDir = USB2811_TRIGDIR_NEGATIVE, it means the trigger level is low. When ATR trigger source signal is lower than trigger level, A/D is in the conversion process, once the ATR trigger source signal is higher than trigger level, A/D conversion will automatically stop, when the trigger source signal is lower than trigger level again, A/D will re-access to the conversion process that is, only converting the data when the trigger source signal is lower than trigger level.

When ADPara.TriggerDir = USB2811_TRIGDIR_POSITIVE, it means the trigger level is high. When ATR trigger source signal is higher than trigger level, A/D is in the conversion process, once the ATR trigger source signal is lower than trigger level, A/D conversion will automatically stop, when the trigger source signal is higher than trigger level again, A/D will re-access to the conversion process, that is, only converting the data when the trigger source signal is higher than trigger level.
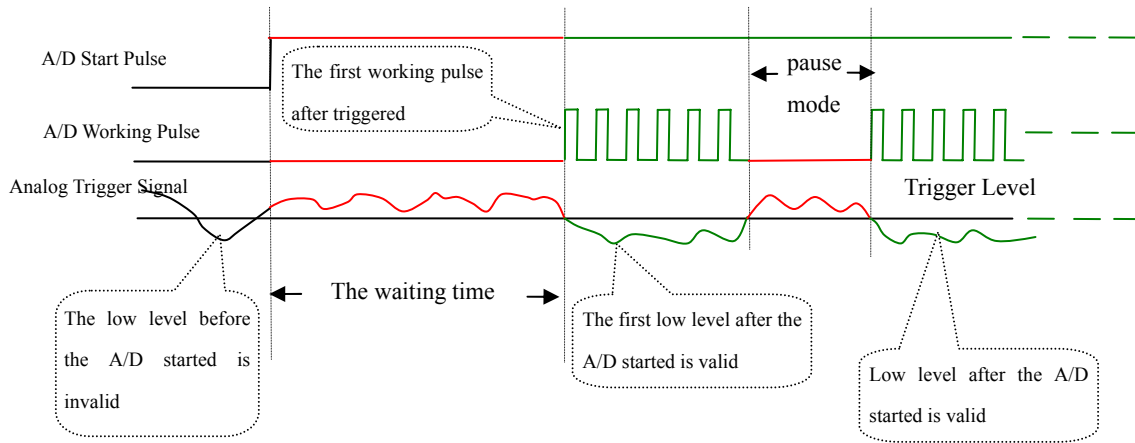
Figure5.3 Digital   Trigger Source，Low Level Trigger

When ADPara.TriggerDir = USB2811_TRIGDIR_POSIT_NEGA, it means A/D can be triggered by positive pulse or negative pulse. The effect is the same as the internal software trigger.

(二)   DTR Trigger

When the trigger signal is the digital signal (standard TTL-level), using the DTR trigger source.

(1) Edge trigger function

Edge trigger is to capture the characteristics of the changes between the trigger source signal and the trigger level signal to trigger A/D conversion.

When ADPara.TriggerDir = USB2811_TRIGDIR_NEGATIVE, choose the trigger mode as the falling edge trigger. That is, when the DTR trigger signal is on the falling edge, A/D will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition.
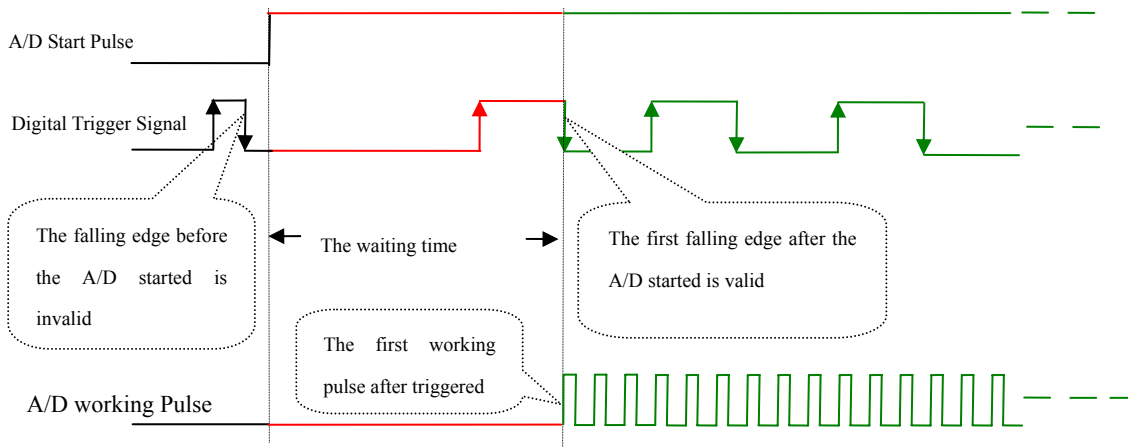

Figure 5.4 Falling edge Trigger

When ADPara.TriggerDir = USB2811_TRIGDIR_POSITIVE, choose the trigger mode as rising edge trigger. That is, when the DTR trigger signal is on the rising edge, A/D will immediately access to the conversion process, and its follow-up changes have no effect on AI acquisition.

When ADPara.TriggerDir = USB2811_TRIGDIR_POSIT_NEGAT, choose the trigger mode as rising or falling edge trigger. That is, when the DTR trigger signal is on the rising or falling edge, A/D will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition. This function can be used in the case that the acquisition will occur if the exoteric signal changes.

（2）**Level trigger function**

Level trigger is to capture the condition that trigger signal is higher or lower than the trigger level to trigger A/D conversion.

When ADPara.TriggerDir = USB2811_TRIGDIR_NEGATIVE, it means the trigger level is low. When DTR trigger signal is in low level, A/D is in the conversion process, once the trigger signal is in the high level, A/D conversion will automatically stop, when the trigger signal is in the low level again, A/D will re-access to the conversion process, that is, only converting the data when the trigger signal is in the low level.

Figure 5.5 High Level Trigger

When ADPara.TriggerDir = USB2811_TRIGDIR_POSITIVE, it means the trigger level is high. When DTR trigger signal is in high level, A/D is in the conversion process, once the trigger signal is in the low level, A/D conversion will automatically stop, when the trigger signal is in the high level again, A/D will re-access to the conversion process, that is, only converting the data when the trigger signal is in the high level.
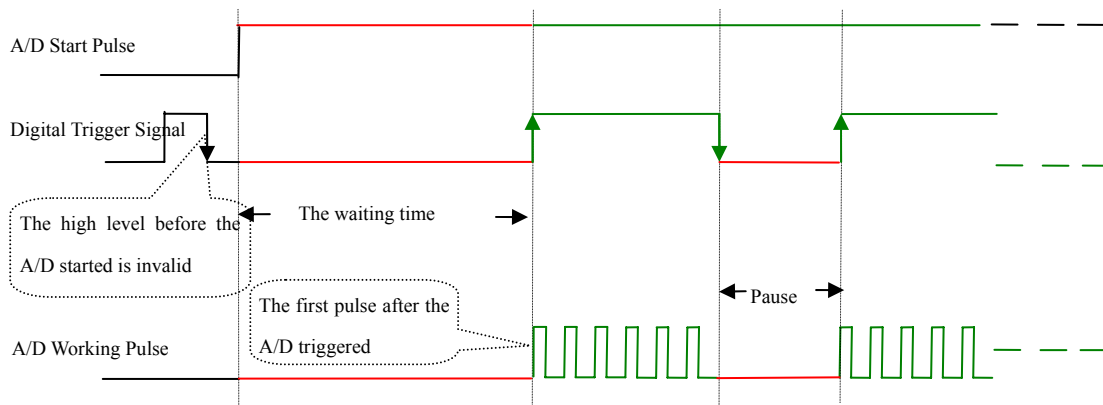
When ADPara.TriggerDir = USB2811_TRIGDIR_POSIT_NEGAT, it means the trigger level is low or high. The effect is the same as the internal software trigger.

Chapter 6 Methods of Using Internal and External Clock Function

6.1 Internal Clock Function

Internal Clock Function refers to the use of on-board clock oscillator and the clock signals which are produced by the user-specified frequency to trigger the A/D conversion regularly. To use the clock function, the hardware parameters ADPara.ClockSouce= USB2811_CLOCKSRC_IN should be installed in the software. The frequency of the clock in the software depends on the hardware parameters ADPara.Frequency. For example, if Frequency = 100000, that means A/D work frequency is 100000Hz (that is, 100 KHz, 10μs /point).

6.2 External Clock Function

External Clock Function refers to the use of the outside clock signals to trigger the A/D conversion regularly. The clock signals are provide by the CLKIN pin of the CN1 connector.   The outside clock can be provided by USB2811 clock output (CLKOUT of CN1), as well as other equipments, for example clock frequency generators. To use the external clock function, the hardware parameters ADPara.ClockSouce = USB2811_CLOCKSRC_OUT should be installed in the software. The clock frequency depends on the frequency of the external clock, and the clock frequency on-board (that is, the frequency depends on the hardware parameters ADPara.Frequency) only functions in the packet acquisition mode and its sampling frequency of the A/D is fully controlled by the external clock frequency.

6.3 Methods of Using AI Continuum and Grouping Sampling Function

6.3.1 Continuum Sampling Function

The continuous acquisition function means the sampling periods for every two data points are completely equal in the sampling process of A/D, that is, completely uniform speed acquisition, without any pause, so we call that continuous acquisition.

To use the continuous acquisition function, the hardware parameters ADPara.ADMode = USB2811_ADMODE_SEQUENCE should be installed in the software. For example, in the internal clock mode, hardware parameters ADPara.Frequency = 100000 (100KHz) should be installed, and 10 microseconds after the A/D converts the first data point, the second data point conversion starts, and then 10 microseconds later the third data point begins to convert, and so on.

The formula for calculating the external signal frequency is as follows:

Under the internal clock mode:

External signal frequency = A/D sampling frequency/（cycle signal points × the total number of sample channels）

External signal cycle = 1 / external signal frequency

Under the external clock mode:

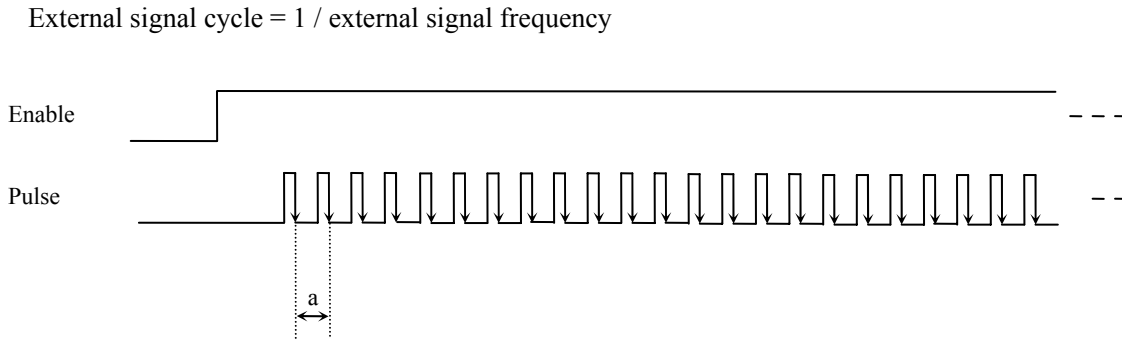External signal frequency = external clock frequency/ (cycle signal points × the total number of sample channels)

External signal cycle = 1 / external signal frequency

Figure 6.1 collecting continuum sampling in internal clock mode

Note: a－sampling cycle

6.3.2 Grouping Sampling Function

Grouping acquisition (pseudo-synchronous acquisition) function refers to the sampling clock frequency conversion among the channels of the group in the AD sampling process, and also a certain waiting time exists between every two groups, this period of time is known as the Group Interval. Loops of group refer to numbers of the cycle acquisition for each channel in the same group. In the internal clock mode and the fixed-frequency external clock mode, the time between the groups is known as group cycle. The conversion process of this acquisition mode as follows: a short time stop after the channels conversion in the group (that is, Group Interval), and then converting the next group, followed by repeated operations in order, so we call it grouping acquisition.

The purpose of the application of the grouping acquisition is that: at a relatively slow frequency, to ensure that all of the time difference between channels to become smaller in order to make the phase difference become smaller, thus to ensure the synchronization of the channels, so we also say it is the pseudo-synchronous acquisition function. In a group, the higher the sampling frequency is, the longer Group Interval is, and the better the relative synchronization signal is. The sampling frequency in a group depends on ADPara. Frequency, Loops of group depends on ADPara.LoopsOfGroup, the Group Interval depend on ADPara. Group Interval.

Based on the grouping function, it can be divided into the internal clock mode and the external clock mode. Under the internal clock mode, the group cycle is decided by the internal clock sampling period, the total number of sampling channels, Loops of group and Group Interval together. In each cycle of a group, AD only collects a set of data. Under the external clock mode, external clock cycle $\geqslant$ internal clock sampling cycle $\times$ the total number of sampling channels $\times$ Loops of group + AD chip conversion time, AD data acquisition is controlled and triggered by external clock. The external clock mode is divided into fixed frequency external clock mode and unfixed frequency external clock mode. Under the fixed frequency external clock mode, the group cycle is the sampling period of the external clock.

The formula for calculating the external signal frequency is as follows:

Under the internal clock mode:
Group Cycle = the internal clock sampling period $\times$ the total number of sample channels $\times$ Loops of group + AD chips

conversion time + Group Interval

External signal cycle = (cycle signal points / Loops of group) × Group Cycle

External signal frequency = 1 / external signal cycle

Under the external clock mode: (a fixed-frequency external clock)

Group Cycle = external clock cycle

External signal cycle = (cycle signal points / Loops of group) × Group Cycle

External signal frequency = 1 / external signal cycle

Formula Notes:

The internal sampling clock cycle = 1 / (AD Para. Frequency)

The total number of sampling channels = AD Para. Last Channel – AD Para. First Channel + 1

  Loops of group == ADPara.LoopsOfGroup

  AD Chips conversion time = see "AD Analog Input Function" parameter

  Group Interval = AD Para. Group Interval

Signal Cycle Points = with the display of the waveform signal in test procedures, we can use the mouse to measure the signal cycle points.

Under the internal clock mode, for example, sample two-channel 0, 1, and then 0 and 1 become a group. Sampling frequency (Frequency) = 100000Hz (cycle is 10μs), Loops of group is 1, Group Interval = 50μs, then the acquisition process is to collect a set of data first, including a data of channel 0 and a data of channel 1. We need 10uS to sample the two data, 20μs to convert the data from the two channels. After the conversion time of an AD chip, AD will automatically cut-off to enter into the waiting state until the 50μs group interval ends. We start the next group, begin to convert the data of channel 0 and 1, and then enter into the waiting state again, and the conversion is going on in this way, as the diagram following shows:
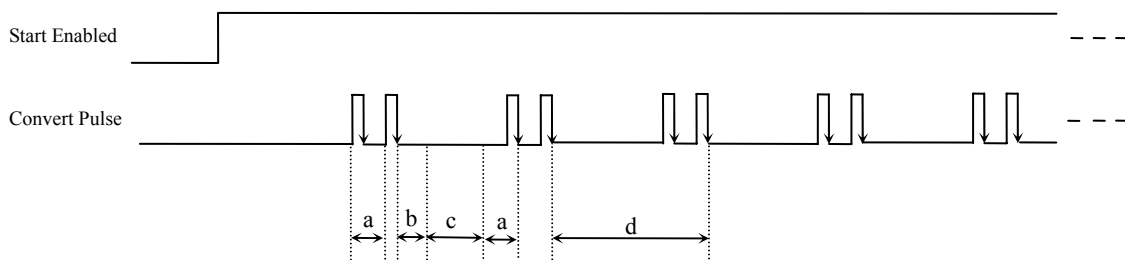

Figure 6.1 Grouping Sampling which grouping cycle No is 1 under the Internal Clock Mode

Note: a— internal clock sample cycle

           b— AD chips conversion time

           c—Group Interval

           d— group cycle

Change the loops of group into 2, then the acquisition process is to collect the first set of data, including two data of channel 0 and two data of channel 1, the conversion order is 0,1,0,1. We need 10μs to sample each of the four data. After the conversion time of an AD chip, AD will automatically stop to enter into the waiting state until the 50μs Group

Interval ends. We start the next group, begin to convert the data of channel 0 and 1, and then enter into the waiting state again, and the conversion is going on in this way, as the diagram following shows:
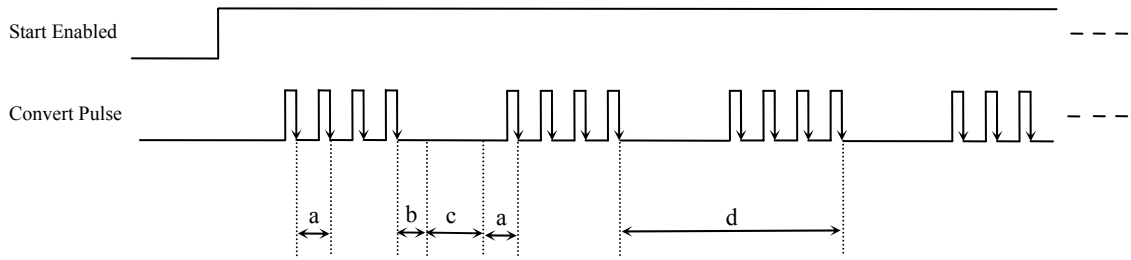

Figure 6.2 Grouping Sampling which grouping cycle No is 2 under the Internal Clock Mode

Notes: a— internal clock sample cycle
                 b— AD chips conversion time
                 c—Group Interval
                 d— group cycle

Under the external clock mode, the requirement is: the external clock cycle ≥ the internal clock sampling period × the total number of sampling channels× Loops of group + AD chip conversion time, otherwise, the external clock appearing in the group conversion time will be ignored.

Under the fixed-frequency external clock mode, for example, when sampling data of two-channel 0, 1, then channel 0 and channel 1 consist of a group. Sampling frequency (Frequency) = 100000Hz (the cycle is 10μs), Loops of group is 2, then the acquisition process is to collect the first set of data, including two data of channel 0 and two data of channel 1, the order of conversion 0,1,0,1, We need 10μs to sample the four data and 40μs to convert of the four data. After the conversion time of an AD chip, AD will automatically stop to enter into the waiting state until the next edge of the external clock triggers AD to do the next acquisition, and the conversion is going on in this way, as the diagram following shows:
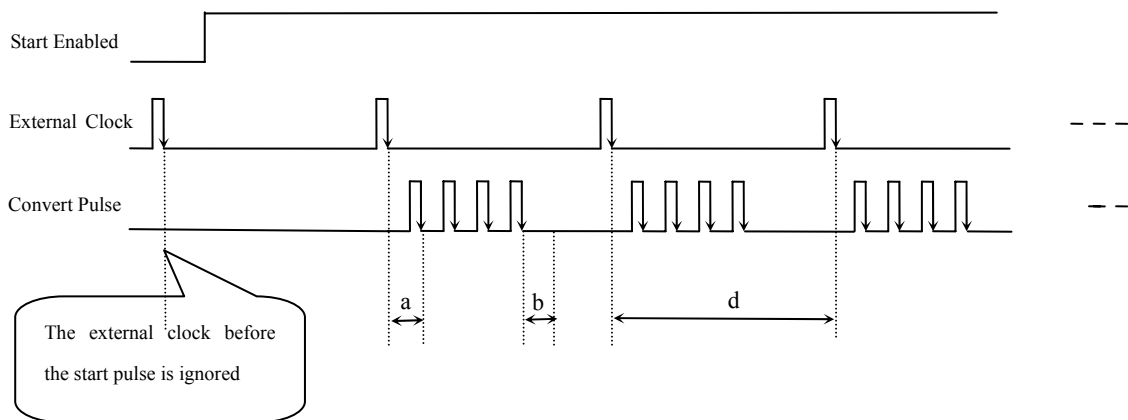

The external clock before the start pulse is ignored

Figure 6.3 Grouping sampling under the fixed frequency external clock mode

Notes: a— internal clock sample cycle
          b—AD chips conversion time
          d—group cycle（external clock cycle）

Under an unfixed-frequency external clock mode, for example, the grouping sampling principle is the same as that of the fixed-frequency external clock mode. Under this mode, users can control any channel and any number of data. Users will connect the control signals with the clock input of the card (CLKIN), set the sampling channels and Loops of group. When there are external clock signals, it will sample the data which is set by users. Because the external clock frequency is not fixed, the size of external clock cycle is inconsistent but to meet: the external clock cycle ≥ the internal clock sampling period × the total number of sampling channels × Loops of group + AD chip conversion time, , otherwise, the external clock edge appearing in the group conversion time will be ignored.
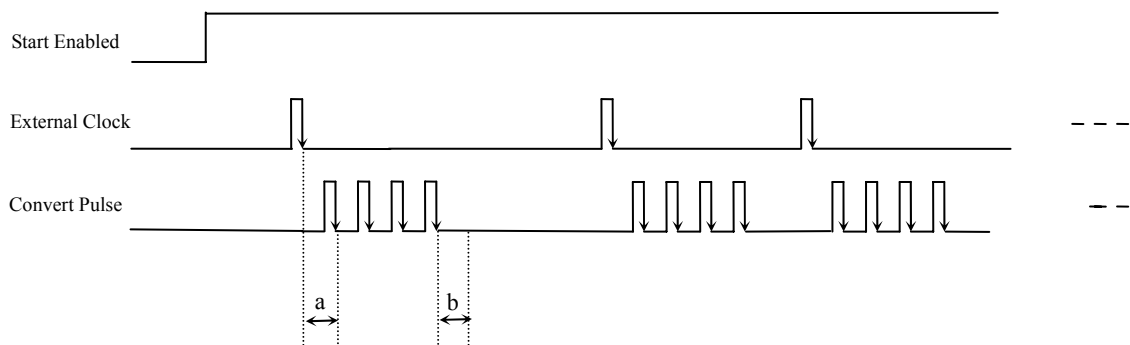

Figure 6.4 Grouping sampling under the not fixed frequency external clock mode

Note: a— internal clock sample cycle
          b—AD chips conversion time

Chapter 7 Timer/Counter Function

Mode 0: Interrupt on terminal count

Under this mode, when given the initial value, if GATE is high level, the counter immediately begins to count by subtracting "1" each time, the counter OUT turns into low level; when the count ends and the count value becomes 0, the counter output OUT becomes and keeps high level until given the initial value or reset. If a counter which is counting is given a new value, the counter will begin to count from the new value by subtracting "1" each time. GATE can be used to control the count, GATE=1 enables counting; GATE=0 disables counting. OUT changes low level to high level can be used as interrupt request.
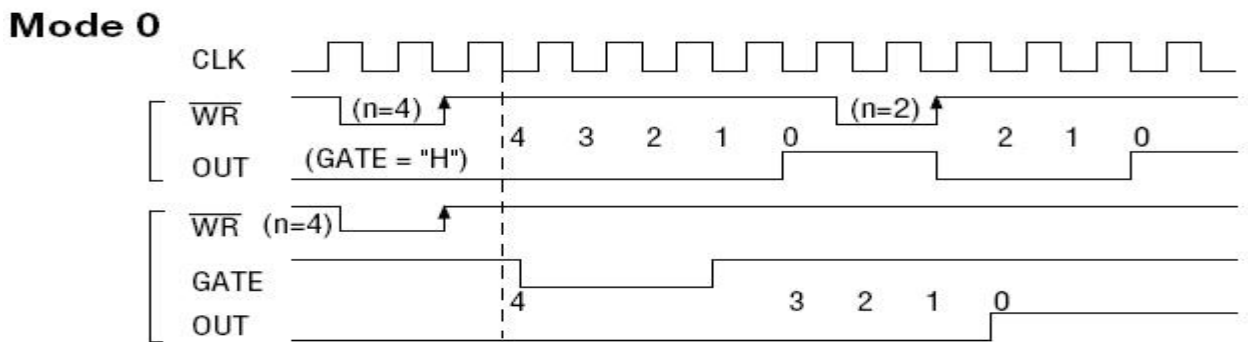
Time diagram is shown in Figure 1.

Figure 1

Mode 1: Hardware retriggerable one-shot

The mode can work under the role of GATE signal. After given the initial count value N, the output OUT becomes high level, the counter begins to count until the appearance of the rising edge of GATE, at this moment the output OUT turns into low level; when the count ends and the count value becomes 0, the output OUT turns into high level, that is, the output one-shot pulse width is determined by the initial count value N. If the current operation does not end and another rising edge of GATE appears, then the current count stops, the counter begins to count from N once again, and then the output one-shot pulse will be widened. When the count reduction of the counter has not yet reached zero, but it is given a new value N1. Only when it is the rising edge of GATE, the counter starts to count from N1.
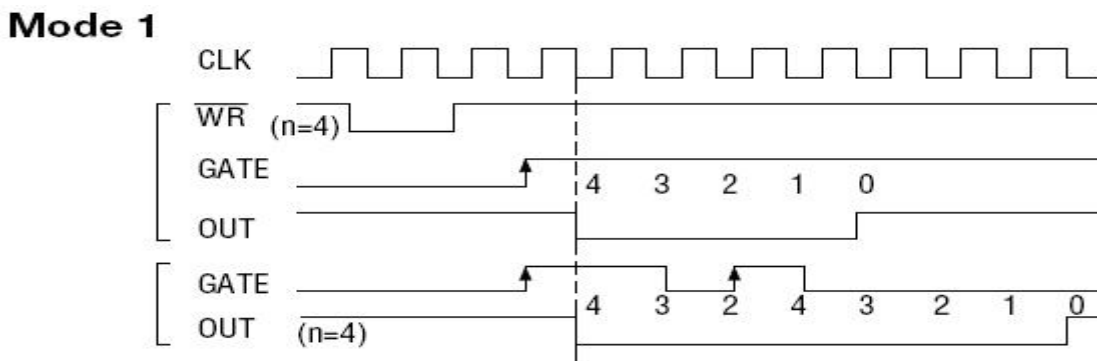
Time diagram is shown in Figure 2.

Figure 2

Mode 2: Rate Generator

Under this mode, the counter is given the initial count value N and begins to count from (N-1), OUT becomes high level. When the count value becomes 0, OUT turns into low level. After a CLK cycle, OUT resumes high level, and the counter automatically load the initial value N and begin to count from (N-1). Thus the output will continue to output a negative pulse, its width is equal to one clock cycle, the clock number between the two negative pulses is equal to the initial value that is given to the counter. GATE=1 enables counting; GATE=0 disables counting. If change the initial count when counting, it will be effective next time.
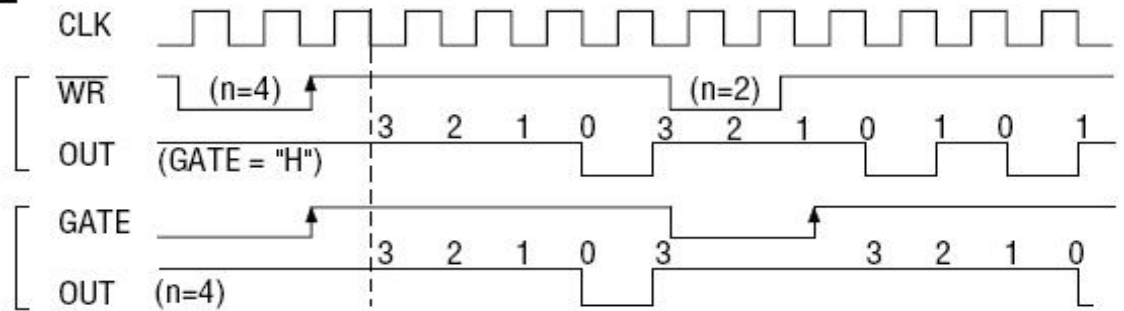
Time diagram is shown in figure 3.

Figure 3

Mode 3: Square wave mode

Similar to Mode 2, the counter is given the initial count value N and begins to count from (N-1). When the signal of GATE is high level, it starts to count, timer/counter begins to count by subtracting "1" each time, more than half the initial count value. The output OUT has remained high level, when the count value is more than half of the initial count value; but the output OUT becomes low level, when the count value is less than half of the initial value. If the initial count value N is an even number, the output is 1:1 square-wave; if the initial count value N is an odd number, the output OUT has remained high level during the previous (n +1)/2 count period; but the output OUT becomes low level during the post (n-1)/2 count period, that is, the high level has one clock cycle more than the low level. If change the initial count when counting, it will be effective next time. When GATE = 0, the count is prohibited, when GATE = 1, the count is permitted. Time diagram is shown in figure 4.
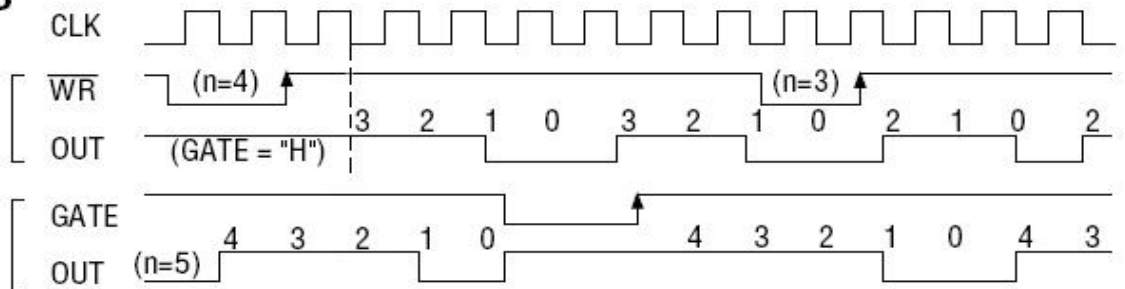

Figure 4

Mode 4: Software triggered strobe

Under this mode, the counter is given the initial count value N and begins to count, the output OUT becomes high level. When the count value becomes 0, it immediately outputs a negative pulse which is equal to the width of one clock cycle. If given a new count value when counting, it will be effective immediately. GATE=1 enables counting; GATE=0 disables counting. Time diagram is shown in figure 5.
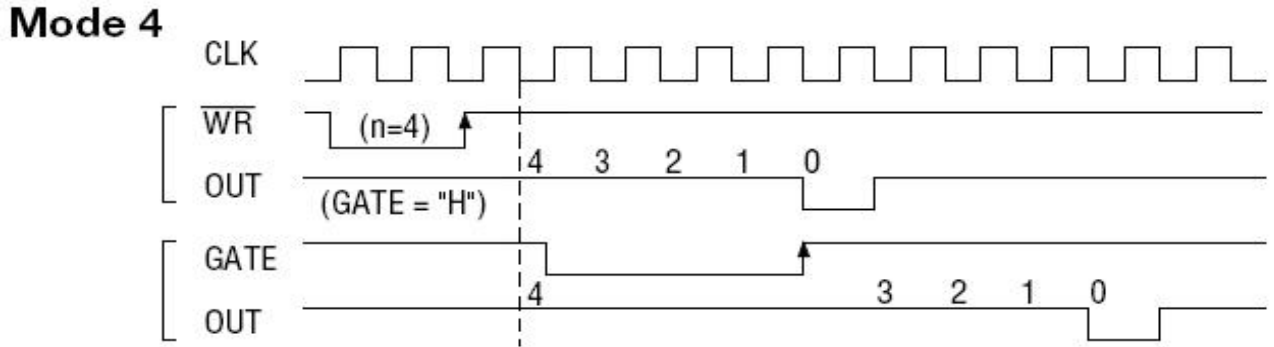

Figure 5

Mode 5: Hardware triggered strobe

Under this mode, when the signal of GATE is on the rising edge, the counter starts to count (so it is called hardware trigger), the output OUT has remained high level. When the count value becomes 0, it outputs a negative pulse which is equal to the width of one clock cycle. And then the rising edge of GATE signal can re-trigger, the counter starts to count from the initial count value again, in the count period, the output has remained high level. When the count reduction of the counter has not yet reached zero, but it is given a new value N1. Only when it is the rising edge of GATE, the counter starts to count from N1. Time diagram is shown in figure 6.
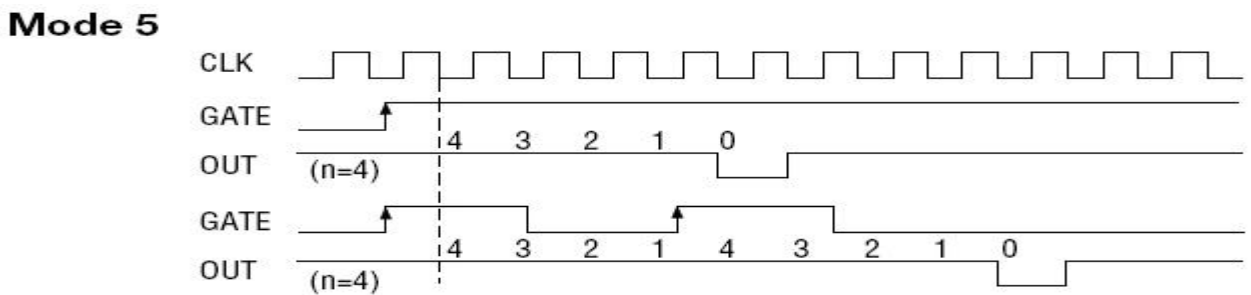

Figure 6

Chapter 8 Notes, Calibration and Warranty Policy

8.1 Notes

In our products' packing, user can find a user manual, a USB2811 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can.

When using USB2811, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of USB2811 module.

8.2 Analog Signal Input Calibration

Every device has to be calibrated before sending from the factory. It is necessary to calibrate the module again if users want to after using for a period of time or changing the input range. In the manual, we introduce how to calibrate USB2811 in ±10V, calibrations of other input ranges are similar.

Prepare a digital voltage instrument which the resolution is more than 5.5 bit, install the USB2811 module, and then power on, warm-up for fifteen minutes.

1) Zero adjustment: select one channel of analog inputs, take the channel AI0for example, connect 0V to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP1 in order to make voltage value is 0.000V or about 0.000V. Zero adjustment of other channels is alike.

2) Full-scale adjustment: select one channel of analog inputs, take the channel AI0 for example, connect 9999.69mV to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP2 in order to make voltage value is 9999.69mV or about 9999.69mV. Full-scale adjustment of other channels is alike.

3) Repeat steps above until meet the requirement.

8.3 Analog Signal Output Calibration

In the manual, we introduce how to calibrate USB2811 in ±5V range, calibrations of other output ranges are similar.

1）Run ART Data Acquisition Measurement Suite in the WINDOWS. Select the analog output test under the menu file operations, select the channel which needs to be calibrated.

2) To set the AO output to 2048, by adjusting the potentiometer RP7 to make AO0~AO3 output 0.000V.

3) To set the AO output to 4095, adjust potentiometer RP6 in order to make AO0 output voltage value is 4997.55mV (adjust potentiometer RP5, Rp4, RP3 to make AO1~AO3 output value is 4997.55mV).

4）Repeat steps above until meet the requirement.

8.4 AO use

In demonstration program, the continuous output interval of waveform output can not be carried out; the main objective is to test the strength of analog output.

8.5 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: www.art-control.com.

2. All ART products come with a limited two-year warranty:

➢   The warranty period starts on the day the product is shipped from ART's factory

➢   For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.

➢   Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:

➢   Damage caused by not following instructions in the User's Manual.

➢   Damage caused by carelessness on the user's part during product transportation.

➢   Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).

➢   Damage from improper repair by unauthorized ART technicians.

➢   Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】; or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the USB card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> USB.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.